

ABSTRACT

A semiconductor device including plural CMOS transistors with first and second transistors sharing a common first gate electrode and third and fourth transistors sharing a common second gate electrode that is adjacent and parallel to the first gate electrode. The first and third transistors share a common n-type channel MOS region and the second and fourth transistors share a common p-type channel MOS region. The semiconductor device has a wire connecting the n-type channel MOS region and the p-type channel MOS region. The wire has a width greater than a distance between the first and second adjacent gate electrodes, and a portion of the wire is disposed right above a portion of at least one of the first and second gate electrodes with an insulating film interposed therebetween.